IEEE 802.16e LDPC Encoder/Decoder Core

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Abstract An optimized hardware-efficient core for implementation of the standard supported LDPC coding is described. The proposed solution has essential performance and implementation advantages over existing convolutional and turbo-convolutional schemes.

1 Introduction

The IEEE 802.16 Telecommunication standard [1] with its amendment to mobile users [2] addressed. We provide an Intellectual Property (IP) for efficient implementation of low-density parity-check (LDPC) forward error correcting (FEC) schemes intended for the IEEE802.16e. The implemented LDPC Encoder/Decoder hardware supports all LDPC codes defined in [2], including 4 code rates, 1/2, 2/3, 3/4 and 5/6, and 19 code lengths ranging from 576 bits to 2304 bits.

2 WiMAX forum

WiMAX (Worldwide Interoperability for Microwave Access) is poised to become a key technical underpinning of fixed, portable and mobile data networks. WiMAX is an implementation of the emerging IEEE 802.16 standard that uses Orthogonal Frequency Division Multiplexing (OFDM) for optimization of wireless data services. OFDM technology uses “sub-carrier optimization,” assigning small sub-carriers (kHz) to users based on radio frequency conditions. This enhanced spectral efficiency is a great benefit to OFDM networks and makes them very well suited to high-speed data connections for both fixed and mobile users. Systems based on the emerging IEEE 802.16 standards are the only standardized OFDM-based Wireless Wide Area Networks (WWAN) infrastructure platforms today.

Service providers will operate WiMAX on licensed and unlicensed frequencies. The technology enables long distance wireless connections with speeds up to 75 megabits per second. (However, network planning assumes a WiMAX base station installation will cover the same area as cellular base stations do today.) Wireless WANs based on WiMAX technology cover a much greater distance than Wireless Local Area Networks (WLAN), connecting buildings to one another over a broad geographic area. WiMAX can be used for a number of applications, including “last mile” broadband connections, hotspot and cellular backhaul, and high-speed enterprise connectivity for businesses.

By 2006, technology based on the IEEE 802.16e standards will be integrated into mobile handsets, portable computers, portable and mobile pda’s enabling applications and services to support movement between WiMAX service areas.

3 Error-correcting coding options in the IEEE802.16e standard

Error-correcting coding is an essential tool for enabling reliable communication. The standard suggests use of the following coding methods:

- Convolutional Code (CC) with mother rate 1/2, defined with the generating polynomial (00171 00133). Additional rates using puncturing are: 2/3, 3/4, 5/6.
- Convolution Turbo Code (CTC) with fundamental rate of 1/3, additional rates using puncturing are: 2/3, 3/4, 5/6.
- Low-density parity check (LDPC) enabling 6 fundamental matrices forming the rates: 1/2, 2A, 2B, 3A, 3B, 5.

CTC and LDPC codes have a clear advantage over CC code in performance. For example, they improve the coding gain by 2–5dB in comparison with CC at the output BER of 10^{-5}. Though the implementation complexity of CTC and LDPC codes is higher than the one of CC, as it will be shown it is still quite modest.

The advantages of LDPC codes over CTC codes are from several aspects, first, the implementation of LDPC codes are relatively light in area space (125 Kgates), the ratio of memory with respect to the total area is distinctively high. Second, unlike the CTC decoder, LDPC codes are patent-free making them a perfect candidate for high volumes low price communication chips. Third, in the IEEE802.16 [1] [2] standard, using CID-less bursts allocations (more efficient network) or when bursts carry large quantities of information, the LDPC has a clear advantage over CTC enabling to encoding codeword length up to 2304 bits compared to 960 bits in the CTC. The performance is 0.75 dB in favor of the LDPC in maximal FEC block transmission conditions.

In the following sections we describe the developed highly-optimized core of LDPC encoder/decoder supporting all the modes defined in the standard and having a very small implementation complexity.
4 Encoder hardware specification

A linear (in the length) time encoding algorithm supporting encoding of 4 code rates and 19 code lengths was implemented. The basic encoder area is 20K gates. The encoder throughput is given in Table I.

![Table I](image)

5 Decoder hardware specification

The architecture of the decoder is scalable in the number of its Processing Units (PU). WiMAX systems will mostly employ Base Stations (BS) and Fixed or Mobile stations (i.e. FS or MS), forming either all-to-one or one-to-all multiple access topology. Based on the access topology a scalable hardware LDPC decoder was developed, supporting both low complexity and modest power consuming MSs and high throughput low latency transport requirements of BSs. The basic decoder area is 125K gates (e.g. 1 PU) in 90 nanometer low-power technology library target with frequency target of 200MHz (synthesizable up to 240 MHz) fully synchronous design using one single clock. The verilog code synthesizable for FPGA and ASIC, proven on Altera evaluation board (e.g. [http://www.altera.com/products/devkits/altera/kit-nios-1S10.html](http://www.altera.com/products/devkits/altera/kit-nios-1S10.html)). For additional PU the basic count of 125K gates will increase by approximately 16K gates per additional PU.

Table II shows the normalized throughput of the decoder for each code matrix defined in [2]. Each number in the table should be multiplied by the factor clock frequency # iterations to obtain the throughput of the payload. The decoder’s scalability is in the number of PUs 1,2,3,4,5 or 6.

![Table II](image)

Table III shows the coding gain loss as a function of the maximal number of iterations supported by the decoder.

The decoder also supports statistical multiplexing, which allows increasing the effective number of iterations that can be performed at the given decoder clock frequency and the number of PU’s by adding additional buffers for decoder input.

Figure 1 shows the performance of the decoder for codeword length of 2304 and 50 iterations.

![Fig. 1](image)

6 Conclusion

We propose a simple core implementing LDPC encoder/decoder supported by the IEEE802.16e standard. This code allows essential improvement of performance of the corresponding communication system with minimal hardware area and power penalties.

References
