

TETRA CTC decoder product brief

TurboBest

1. Introduction3
2. Block diagram3
3. Features.....3
4. Throughput4
5. Ordering information4
6. References4

Figure 1 - CTC decoder block diagram3

1. Introduction

The TETRA CTC decoder designed to meet the TETRA (Terrestrial Trunked Radio) and TEDS (TETRA Enhanced Data Service) specification [\[Ref 1\]](#).

CTC encoder and decoder enable an extremely effective way of transmitting data reliably over noisy data channels.

2. Block diagram

Below is the CTC decoder block diagram.

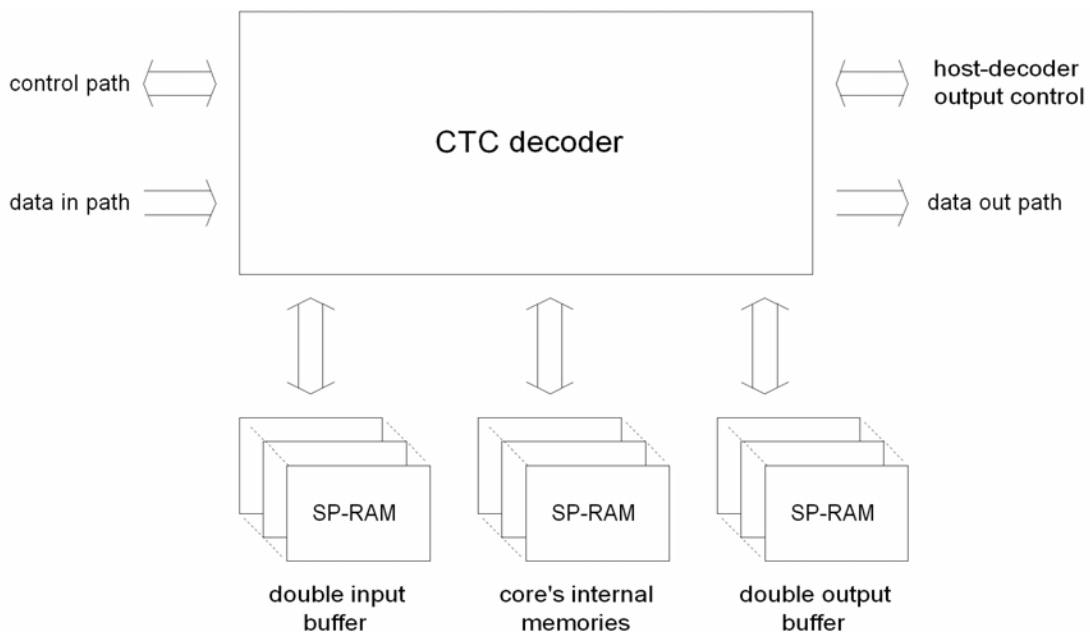


Figure 1 - CTC decoder block diagram

3. Features

- Implements the TETRA specification [\[Ref 1\]](#)
- Up to 6114 bits block size range supported.
- Core contains the full interleaver
- Dynamically selectable number of iterations 1–32, in half iteration resolution.
- Parametric soft input width (pre compile).
- Optional early termination mechanism is available to support power saving and higher statistical throughput.
- Matlab bit exact model is available.

4. Throughput

The throughput is function of the technology target.

FPGA is able to reach ~190MHz clock frequency with throughput of up to 18.7Mbps with 5 decoder iterations.

ASIC technology is able to reach 500-700MHz clock frequency with throughput of more than 50Mbps.

5. Ordering information

For more information please contact us at info@turbobest.com

You can visit our Web site at <http://www.turbobest.com>

We are offering hardware and software free evaluations.

6. References

1. ETSI, “Terrestrial Trunked Radio (TETRA); Voice plus Data (V+D); Part 2: Air Interface (AI),” ETSI EN 300 392–2 V3.4.1, (2010-08).